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|  **UNIVERSITY OF NIŠ** |
| **Course Unit Descriptor** | **Faculty** | Faculty of Electronic Engineering, Niš |
| **GENERAL INFORMATION** |
| Study program  | Electrical Engineering and Computing |
| Study Module (if applicable) | Electronic Devices and Microsystems |
| Course title | Digital System Architecture |
| Level of study | ☐Bachelor ☐ Master’s ☐ Doctoral |
| Type of course |  Obligatory X Elective |
| Semester  | ☐Autumn☐ Spring |
| Year of study  | IV |
| Number of ECTS allocated | 5 |
| Name of lecturer/lecturers | Đorđević Lj. Goran |
| Teaching mode | ☐Lectures ☐Group tutorials ☐ Individual tutorials☐Laboratory work ☐ Project work ☐ Seminar☐Distance learning ☐ Blended learning ☐ Other |
| **PURPOSE AND OVERVIEW (max. 5 sentences)** |
| The course objective is to teach students with basic principles of digital systems design with emphasis on a hardware description language approach.At the end of this course, students are expected to use techniques, skills and modern engineering tools for digital systems design including: a) simulation of hardware description language-based digital systems designs through electronic design automation software; b) synthesize digital systems designs suitable for implementation on programmable device technologies. |
| **SYLLABUS (brief outline and summary of topics, max. 10 sentences)** |
| Introduction to principles of digital circuits and systems design. Overview of design implementation technologies. Programmable device technologies: PLA, CPLD, and FPGA, design flow, electronic design automation software and development tools. Introduction to VHDL: VHDL code structure, design styles, VHDL design units. Lexical elements and objects: data types, signals, variables and arrays, data conversion, operators and attributes. Concurrent statements: WHEN, SELECT, and GENERATE, conceptual diagrams, and synthesis of concurrent code. Sequential code: process, sequential statements IF, CASE, and LOOP, synthesis of sequential code, sequential code for combinational and sequential circuits. Finite state machines: state diagram, algorithmic state machines, state coding, VHDL design of finite state machine. Package and components: statements PACKAGE and COMPONENT, structural and hierarchical design. Functions and procedures. |
| **LANGUAGE OF INSTRUCTION** |
| ☐Serbian (complete course) ☐ English (complete course) ☐ Other \_\_\_\_\_\_\_\_\_\_\_\_\_ (complete course)☐Serbian with English mentoring ☐Serbian with other mentoring \_\_\_\_\_\_\_\_\_\_\_\_\_\_ |
| **ASSESSMENT METHODS AND CRITERIA** |
| **Pre exam duties** | **Points** | **Final exam** | **points** |
| **Activity during lectures** | **10** | **Written examination** | **30** |
| **Practical teaching** | **10** | **Oral examination** | **20** |
| **Teaching colloquia** | **30** | **OVERALL SUM** | **100** |
| **\*Final examination mark is formed in accordance with the Institutional documents** |